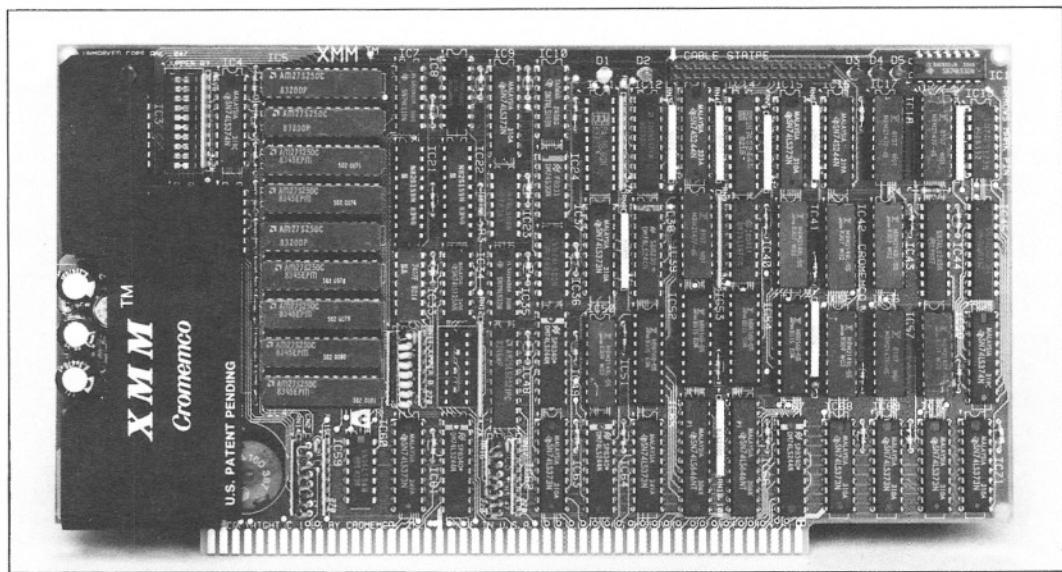


MODEL XMM
Memory Manager Board



FEATURES

- Logical-to-Physical Address mapping of 16 megabytes in 32 segments of 128 pages of 4K bytes
- Supports 15 resident process tables
- High speed Translation Look-aside Buffer
- Demanded pages loaded automatically by hardware
- Separate user and supervisor address spaces
- 6 access modes; checked by hardware
- Single instruction context switch
- Virtual memory support via "resident", "referenced", and "modified" bits.

The Cromemco Memory Manager board, model XMM, operates in conjunction with X-series processor and memory boards to form a high-speed, memory-mapped computer system. The XMM translates the memory references made by the software into specific addresses for main memory. This process, known as logical-to-physical address translation, occurs on every memory cycle. In addition to translating the addresses, the XMM checks every reference to verify that it is "legal"; this allows the operating system to define access privileges and thus to protect main memory from unauthorized examination or alteration. This process also provides bounds to contain runaway programs and therefore tends to isolate each program from other programs on the machine.

The XMM offers memory management features typically found only on mainframes or large minicomputers, including a high-speed Translation Look-aside Buffer (TLB) which is maintained in 4096 words of high-speed (55 nsec) on-board memory. The TLB contains the information which maps the 16 megabyte address space of the current user into 4096 byte pages; this information is automatically updated

by on-board DMA. A separate high-speed lookup table stores the context information, allowing any of the fifteen resident process entries to be selected with a single instruction "context switch". A "demand-paged" algorithm is used to replace entries in the TLB after a context switch; the first time a page is referenced, the hardware detects that it has no entry in the TLB for the page, and the appropriate information is fetched from main memory. The entire operation is transparent to the user and the operating system. A significant speed advantage is gained over less sophisticated schemes in which the entire table is pre-loaded by software at each context switch.

Virtual memory is supported by the XMM through its ability to denote which pages have been referenced or modified by a software process. The hardware sets a "referenced" bit each time the page is referenced, and the operating system can periodically scan the bits to see which pages have been used. For each page which has been referenced, the current time is recorded and the bit is cleared. When it later becomes necessary to remove pages from memory, the system can examine the record of times and remove those pages which have been least recently used. Once a decision has been made to remove a page from memory, it is necessary to know whether it has been modified since it was last read from disk. The "modified" bit is used to signify that a page has been changed since it was read from the disk, and must be re-written. Pages which do not have the modified bit set are not re-written, since the original copy on the disk is still valid.

The advanced design on the XMM includes a multi-layer printed circuit board for reliable operation, and a switch-mode power supply for highly efficient power conversion. Also included is a diagnostic mode of operation with indicator lamps to monitor the operation of the board.

TECHNICAL SPECIFICATIONS

Physical Address Span:	Segment table:
16,777,216 bytes	15 entries
Logical Address Span:	Translation table:
16,777,216 (with 68010 processor)	4096 entries
65,536 (with Z-80 processor)	Context switch:
Segments:	Single instruction
32	Page load time:
Pages:	1.5 microsecond
128	On-board memory:
Page Size:	5K bytes 45 nsec RAM
4096 bytes	8K bytes 55 nsec RAM
Access checks:	Power Requirements:
Supervisor	+ 18 volts 1.6 amp
User	Operating Environment:
Code	0° to 55°C
Data	
Read	
Write	

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